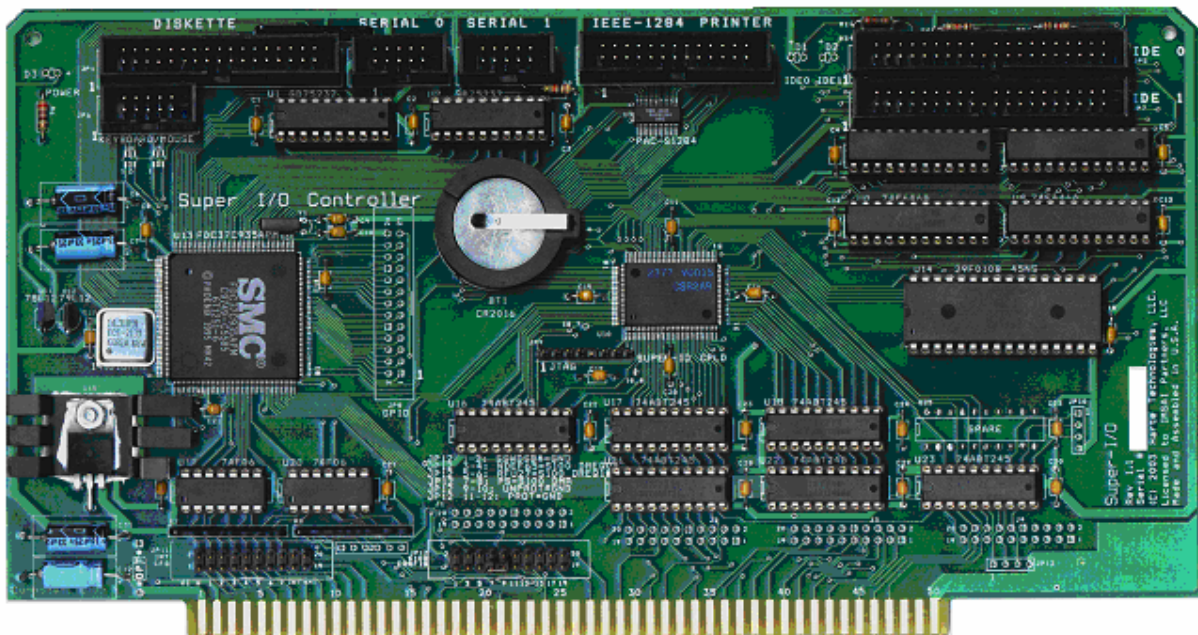


S-100 Super I/O Controller

External Architecture Specification

Revision 1.2
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First Edition

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Revision History			
1.0	11/23/2003	HMH	Board etch revision 1.1, CPLD Version 1.0
1.2	2/6/2004	HMH	Board etch revision 1.1, FINT wire mod and IDE Mux trace cuts. CPLD Version 1.2. See revision 1.2 schematics for details.

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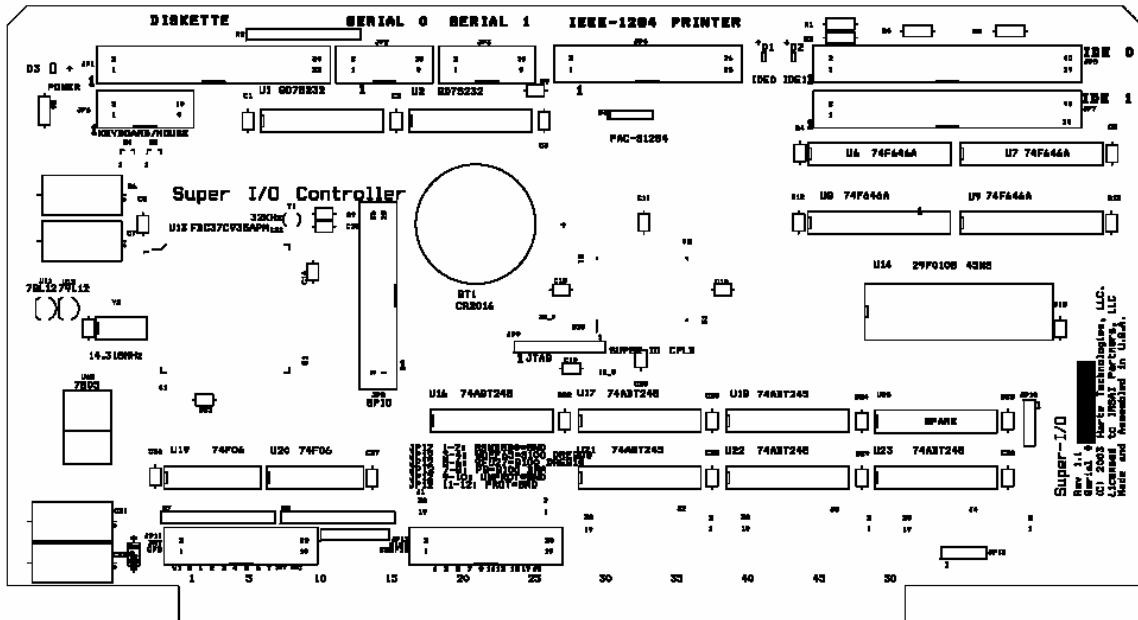
1. Introduction

The HarteTec Super I/O Controller Board provides a complete I/O subsystem for the IEEE-696 bus. The Super I/O Controller supports 8-bit address decoding for compatibility with the original IMSAI 8080 and other S-100 bus systems as well as enhanced 16-bit address decoding supported by the MPU-C processor board in the IMSAI Series Two. The Super-I/O controller also supports DMA for floppy disk access via the MPU-C processor board on-board DMA controller. The Super-I/O controller does not support IEEE-696 Temporary Master Access (TMA.)

The Super I/O Controller provides the following features:

- Standard Microsystems Corporation (SMsC) FDC37C935APM Super I/O Controller.
- Support for two Floppy Diskette drives, in any combination:
- 3.5-inch 2.88MB, 1.44MB, 720KB.
- 5.25-inch 1.2MB, 360KB, DS/HD, DS/DD, SS/DD, SS/SD.
- 8-inch Single or Double-Density.
- Two NS16550-compatible UARTS.
- One IEEE-1284-compatible parallel port.
- PS/2-compatible keyboard/mouse controller.
- Two independent IDE channels supporting up to two IDE devices each.
- Battery backed real-time clock/calendar with non-volatile RAM.
- 128KB FLASH memory with banked memory support and selectable window size.

Harte Technologies products are shipped factory assembled and supplied with a 90-day warranty on parts and labor UNLESS specified otherwise.



2. Theory of Operation

The S-100 Super-I/O Controller is comprised of several sections.

2.1. Power Supply

The Super-I/O Controller takes unregulated input voltages from the S-100 Bus and regulates them to the levels required on-board. All logic on the Super-I/O controller operates from a +5VDC supply, which is generated by U15, and LT323AT 5V 3A regulator. The RS-232 serial port transceivers require +/-12V supply which is provided through U11 and U12, which are 78L12 and 79L12 devices respectively.

2.2. S-100 Bus Buffering

S-100 bus buffering consists of six 74ABT245 octal bus transceivers. These transceivers were chosen for their high-speed, high-drive, and low-power properties. Each bus transceiver has its direction control input hardwired for the appropriate direction. Address and control signal buffers are always enabled. The Super-I/O CPLD controls the enables for the Data-In and Data-Out bus buffers.

2.3. S-100 Bus Bridge

The interface between the S-100 bus and the Super-I/O on-board peripherals is facilitated by an S-100 Bus to ISA Bus Bridge. This bridge is implemented in a Lattice Semiconductor M4A5 CPLD. This bridge takes care of decoding S-100 bus cycles and converting them to standard RD#/WR#/CS# signals. The S-100 Bus Bridge also takes care of I/O port and memory address decoding, FLASH memory mapping, and together with U6-U9 (74ABT646) implements the dual IDE interface. The S-100 Bus Bridge also provides memory and I/O wait-states. One wait-state for memory and I/O cycles is provided by default. More wait states may be added by reprogramming the CPLD.

2.4. High-Density Floppy Disk Interface

The floppy disk interface is largely provided inside the SMsC Super-I/O Controller; however, for operation with high-density floppy diskettes at 4MHz or less, and for reliable operation with low-density diskettes at 2MHz or less, extra logic is included in the Super-I/O CPLD which synchronizes the floppy disk controller FIFO with the host CPU. This synchronization relieves the need for the CPU to poll the floppy disk registers during data transfer. In order to take advantage of this synchronization mechanism, floppy disk controller interrupts must be enabled on INT10 in the FDC37C93APM configuration registers. Software which reads and writes data to the floppy disk controller FIFO uses address 09Dh instead of address 095h when transferring data to/from the FIFO. By using register 9Dh, wait-states are inserted into each I/O cycle until the floppy disk controller FIFO is ready for data.

3. Hardware Specification

3.1. Super I/O On-Board Registers

Device	I/O Range	FDC37C935APM Configured for Address:
IEEE-696 Slave Bridge	80-83	N/A
Parallel Port	88-8F	0x308-30F
Floppy	90-97	0x310-317
Floppy (DMA)	98-9F	N/A
Serial 0	A0-A7	0x320-327
Serial 1	A8-AF	0x328-32F
IDE0/1	B0-B7	N/A
Keyboard/Mouse Configuration	E0,E4 F0,F1	0x60, 64 0x370 (CFGEN bit in BSR register must be set.)
Real-Time Clock	F0,F1	0x70, 71 (CFGEN bit in BSR register must be cleared.)
GPR	F2	
GPW	F3	
Access.BUS	F4-F7	

Figure 1: S-100 Super-I/O Board on-board Registers

IEEE-696 Slave Bridge Registers

	7	6	5	4	3	2	1	0
Mnemonic	CFGEN	-	-	BANK[4]	BANK[3]	BANK[2]	BANK[1]	BANK[0]
Reset	1	0	0	0	0	0	0	0
R/W	R/W	R/O	R/O	R/W	R/W	R/W	R/W	R/W

Figure 2: Bank Select Register, 80H (BSR)

CFGEN: This bit allows software to access the FDC37C935APM configuration ports located at I/O address 0F0h-0F1h. When this bit is set, the FDC37C935APM can be put into configuration mode by writing 055h to I/O port 0F0h. Subsequent writes to I/O ports 0F0h and 0F1h are needed to configure the FDC37C935APM. When this bit is cleared, I/O accesses to port 0F0h and 0F1h access the Super I/O real-time clock registers instead of the configuration ports.

BANK[4:0]: These bits select the current addressed bank of FLASH. Valid bank numbers range from 0 to 31. Bank 00h is selected upon RESET.

	7	6	5	4	3	2	1	0
Mnemonic	-	-	-	-	-	WSZ[2]	WSZ[1]	WSZ[0]
Reset	0	0	0	0	0	0	0	1
R/W	R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W

Figure 3: Window Size Register, 81H (WSR)

WSZ[2:0]: These bits select the Window Size for the FLASH according to the following table:

WSZ[2:0]	Window Size	# of Banks	
0	FLASH Disabled	0	
1	4K	32	
2	8K	16	
3	16K	8	
4	32K	4	
5	64K	2	
6	128K	1	

Figure 4: Window Size Selection Bit Definition

	7	6	5	4	3	2	1	0
Mnemonic	A19	A18	A17	A16	A15	A14	A13	A12
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Figure 5: FLASH Base Address Register, 82H (BAR)

A[19:12]: These register selects the base address of the FLASH device in the memory map. When a 4K window size is selected, all address bits in the BAR must match the current memory cycle address in order for the FLASH to be selected. When a 128K window size is selected, only bits A[19:17] are compared.

	7	6	5	4	3	2	1	0
Mnemonic	-	-	-	-	-	-	-	IDE_SEL
Reset	0	0	0	0	0	0	0	0
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W

Figure 6: IDE Multiplex Register, 83H (MUX)

IDE_SEL: This bit selects whether the Primary or Secondary IDE controller is selected. The registers for the selected controller appear at I/O addresses 0B0h-0B7h. When this bit is clear, the Primary IDE Controller (IDE 0) is selected. When this bit is set, the Secondary IDE Controller (IDE 1) is selected.


3.2. Hardware Configuration Options

Interrupt Configuration Jumper Block (JP11)

Jumper Block JP11	Description (When jumper is inserted)	Notes	
1-2	SMsC IRQ10 maps to IEEE-696 VI0	[DEFAULT]	
3-4	SMsC IRQ9 maps to IEEE-696 VI1	[DEFAULT]	
5-6	SMsC IRQ8 maps to IEEE-696 VI2	[DEFAULT]	
7-8	SMsC IRQ7 maps to IEEE-696 VI3	[DEFAULT]	
9-10	SMsC IRQ6 maps to IEEE-696 VI4	[DEFAULT]	
11-12	SMsC IRQ5 maps to IEEE-696 VI5	[DEFAULT]	
13-14	SMsC IRQ4 maps to IEEE-696 VI6	[DEFAULT]	
15-16	SMsC IRQ3 maps to IEEE-696 VI7	[DEFAULT]	
17-18	SMsC IRQ3 maps to IEEE-696 INT		
19-20	SMsC IRQ3 maps to IEEE-696 NMI		

Note: odd pins on Jumper block JP11 may be used as testpoints to their respective S-100 bus signals. Odd pins are connected to the S-100 bus, while even pins are connected to the Super I/O local bus.

S-100 Bus Configuration Jumper Block (JP12)

Jumper Block JP12	Description (When jumper is inserted)	Notes		
1-2	S100 SSWDSB# tied to ground.	[DEFAULT]		
3-4	IEEE-696 NDEF65 is S100_DREQ0	[DEFAULT] (S2 Specific)		
5-6	IEEE-696 NDEF66 is S100_DREQ1	[DEFAULT] (S2 Specific)		
7-8	S100 PS is S100_DMA	[DEFAULT] (S2 Specific)		
7-9	L_DMA tied to ground.	Necessary when the Super I/O board is used in a system without DMA.		
9-10	UNPROT tied to ground.	[DEFAULT]		
11-12	PROT tied to ground	[DEFAULT]		
14	SS Test Point			
16	RUN Test Point			
18	RFU27 Test Point			
20	PINTE Test Point			
<p>Note: even pins on Jumper block JP12 may be used as testpoints to their respective S-100 bus signals. Even pins are connected to the S-100 bus, while odd pins are connected to the Super I/O local bus.</p>				

Super-I/O Controller Connector Pinouts

Signal	Description	Direction	2x17 Header Pin Number	
DRV DEN0		In	2	
N/C	No Connect		4	
DRV DEN1		In	6	
INDEX#	index pulse	In	8	
MTR_EN0#	Motor 0 Enable	Out	10	
DRVSEL0#	Drive Select 0	Out	12	
DRVSEL1#	Drive Select 1	Out	14	
MTR_EN1#	Motor 1 Enable	Out	16	
DIR#	Step Direction	Out	18	
STEP#	Step Pulse	Out	20	
WDATA#	Write Data	Out	22	
WGATE#	Write Gate	Out	24	
TRACK0#	Track 0 signal	In	26	
WPROT#	Write Protect	In	28	
MEDIA_ID0	Media ID bit 0	In	29	
RDATA#	Read Data	In	30	
HDSEL#	Head Select	Out	32	
MEDIA_ID1	Media ID bit 1	In	33	
DSK_CHG#	Disk Change	In	34	
GND	Ground	-	Unlisted pins	

Figure 7: JP1 - Super-I/O Floppy Drive Connector

Signal	Description	Direction	MPU-C 2x5 Header Pin Number	DB9-M Connector on Cabinet	DB25-M Connector on Cabinet	
DCD	Data Carrier Detect	In	1	1	8	
DSR	Data Set Ready	In	2	6	6	
RxD	Receive Data	In	3	2	3	
RTS	Request to Send	Out	4	7	4	
TxD	Transmit Data	Out	5	3	2	
CTS	Clear to Send	In	6	8	5	
DTR	Data Terminal Ready	Out	7	4	20	
RI	Ring Indicator	In	8	9	22	
GND	Signal Ground	-	9	5	7	
-	Key	-	10	-	-	

Figure 8: JP2, JP3 - Super-I/O Serial Ports 0 and 1.

Signal	Description	Direction	MPU-C 2x5 Header Pin Number	DB25-F Connector on Cabinet	Centronics 36Pin	
STROBE#	Strobe Signal	Out	1	1	1	
AUTOFD#	Auto Linefeed	Out	2	14	14	
DATA0	Data Line 0	I/O	3	2	2	
ERROR#	Error	In	4	15	32	
DATA1	Data Line 1	I/O	5	3	3	
INIT	Initiate Output	Out	6	16	31	
DATA2	Data Line 2	I/O	7	4	4	
SELECTIN#	Printer Select	Out	8	17	36	
DATA3	Data Line 3	I/O	9	5	5	
GND	Signal Ground	-	10	18	16	
DATA4	Data Line 4	I/O	11	6	6	
GND	Signal Ground	-	12	19	17	
DATA5	Data Line 5	I/O	13	7	7	
GND	Signal Ground	-	14	20	19	
DATA6	Data Line 6	I/O	15	8	8	
GND	Signal Ground	-	16	21	20	
DATA7	Data Line 7	I/O	17	9	9	
GND	Signal Ground	-	18	22	21	
ACK#	Acknowledge	In	19	10	10	
GND	Signal Ground	-	20	23	22	
BUSY	Busy	In	21	11	11	
GND	Signal Ground	-	22	24	23	
PE	Paper Error	In	23	12	12	
GND	Signal Ground	-	24	25	24	
SELECT	Printer Selected	In	25	13	13	
-	Key	-	26	-	-	
GND	Signal Ground	-	-	-	25	
GND	Signal Ground	-	-	-	26	
GND	Signal Ground	-	-	-	27	
GND	Signal Ground	-	-	-	28	
GND	Signal Ground	-	-	-	28	
GND	Signal Ground	-	-	-	29	
GND	Signal Ground	-	-	-	30	
GND	Signal Ground	-	-	-	33	

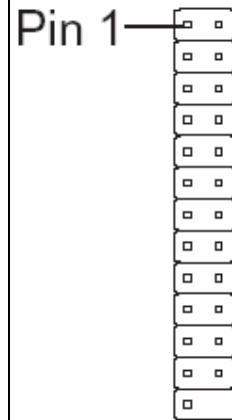


Figure 9: JP4 - Super-I/O Parallel Port

Signal	Description	Direction	2x20 Header Pin Number		
RESET*	Reset HD	Out	1		
GND	Ground	-	2		
HD7	HD data 7	In/Out	3		
HD8	HD data 8	In/Out	4		
HD6	HD data 6	In/Out	5		
HD9	HD data 9	In/Out	6		
HD5	HD data 5	In/Out	7		
HD10	HD data 10	In/Out	8		
HD4	HD data 4	In/Out	9		
HD11	HD data 11	In/Out	10		
HD3	HD data 3	In/Out	11		
HD12	HD data 12	In/Out	12		
HD2	HD data 2	In/Out	13		
HD13	HD data 13	In/Out	14		
HD1	HD data 1	In/Out	15		
HD14	HD data 14	In/Out	16		
HD0	HD data 0	In/Out	17		
HD15	HD data 15	In/Out	18		
GND	Ground	-	19		
N/C	No Connect	-	20		
AEN	Address Enable	Out	21		
GND	Ground	-	22		
IOW*	I/O Write	Out	23		
GND	Ground	-	24		
IOR*	I/O Read	Out	25		
GND	Ground	-	26		
IOCHRDY	I/O Channel Ready	In	27		
BALE	Bus Address Latch Enable	Out	28		
N/C	No Connect	-	29		
GND	Ground	-	30		
IRQ	Interrupt Request	In	31		
IOCS16*	16 bit transfer	In	32		
A1	Address 1	Out	33		
GND	Ground	-	34		
A0	Address 0	Out	35		
A2	Address 2	Out	36		
HCS0*	HD Select 0	Out	37		
HCS1*	HD Select 1	Out	38		
LED	HDD activity LED (-)	In	39		
GND	Ground	-	40		

Figure 10: JP5,7 - Super-I/O IDE Channel 0 and 1 Connectors

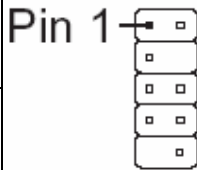


Signal	Description	Direction	MPU-C 2x5 Header Pin Number		6-Pin Female Mini- DIN on Chassis	
-	No Connect	-	1		-	
KDATA	Keyboard Data	I/O	2		1	
KCLK	Keyboard Clock	O	3		5	
-	Key	-	4		2,6	
KGND	Keyboard Ground	O	5		3	
-	No Connect	-	6		-	
MDATA	Mouse Data	I/O	7		1	
MCLK	Mouse Clock	O	8		5	
-	No Connect	-	9		2,6	
MGND	Mouse Ground	-	10		3	

Figure 11: JP6 - Super-I/O PS/2 Keyboard/Mouse Port

Signal	Description	Direction	13x2 Header Pin Number		
GPIO10	SMsC GPIO 10	In/Out	1		
GPIO11	SMsC GPIO 11	In/Out	2		
GPIO12	SMsC GPIO 12	In/Out	3		
GPIO13	SMsC GPIO 13	In/Out	4		
GPIO14	SMsC GPIO 14	In/Out	5		
GPIO15	SMsC GPIO 15	In/Out	6		
GPIO16	SMsC GPIO 16	In/Out	7		
GPIO17	SMsC GPIO 17	In/Out	8		
GPIO20	SMsC GPIO 20	In/Out	9		
GPIO21	SMsC GPIO 21	In/Out	10		
GPIO22	SMsC GPIO 22	In/Out	11		
GPIO23	SMsC GPIO 23	In/Out	12		
GPIO24	SMsC GPIO 24	In/Out	13		
GPIO25	SMsC GPIO 25	In/Out	14		
GPIO60	SMsC GPIO 60	In/Out	15		
GPIO61	SMsC GPIO 61	In/Out	16		
GPIO62	SMsC GPIO 62	In/Out	17		
GPIO63	SMsC GPIO 63	In/Out	18		
GPIO64	SMsC GPIO 64	In/Out	19		
GPIO65	SMsC GPIO 65	In/Out	20		
GPIO66	SMsC GPIO 66	In/Out	21		
GPIO67	SMsC GPIO 67	In/Out	22		
GPIO53	SMsC GPIO 53	In/Out	23		
GPIO54	SMsC GPIO 54	In/Out	24		
GND	Ground	-	25		
GND	Ground	-	26		

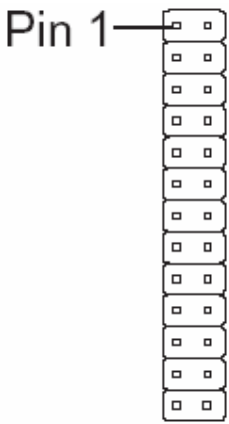


Figure 12: JP8 - Super-I/O GPIO Header Pinout

Please note: The GPIO pins provided on the S-100 Super I/O Controller are directly connected to the SMsC Super I/O controller. They are not buffered and have no additional protection, so extreme caution should be used when using these pins. These pins can sink only 4mA and source only 2mA.

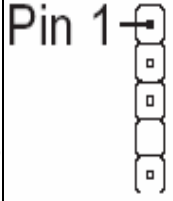
Signal	Description	Direction	1x8 Header Pin Number		
TRST#	Test Mode Reset	In	1	See Lattice Semiconductor M4A5 Datasheet for more information. (http://www.latticesemi.com)	
TDO	JTAG Data Out	Out	2		
TDI	JTAG Data In	In	3		
ENABLE#	Enable	In	4		
-	Key	-	5		
TMS	Test Mode Select	In	6		
GND	Signal Ground	-	7		
TCK	JTAG Clock	In	8		

Figure 13: JP9 - Super-I/O ISP Download Port

4. Software Interface

Please refer to the Super-I/O User's Guide for details.

5. References

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2. CP/M 3.0 System Guide, Digital Research, 1983.
3. Technical Reference, Personal Computer AT, International Business Machines Corporation, September, 1985. (6139362)